Accurate Sheet Resistance Measurement on Ultra-Shallow Profiles

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ABSTRACT

The accurate and reliable characterization of the sheet resistance of ultra-shallow (USJ) profiles is a key issue in the development of future CMOS technologies. Typically, conventional means, such as in-line four point probe measurements, have a limited accuracy due to the substrate contribution resulting from too much probe penetration, especially in the presence of highly doped underlying layers (such as well/halo-profiles). In this work, a series of advanced Boron doped layers have been grown with Chemical Vapor Deposition (CVD) and have been characterized with a large variety of state-of-the art non-penetrating/non-contact sheet resistance tools. The highly doped CVD layers have thicknesses ranging from 132 nm down to 2 nm, and have been grown both on medium and lowly doped substrates. The sheet resistance values are measured using the non-penetrating, non-destructive, elastic metal four point probe (EMP) from Solid State Measurements, the micro four point probe (M4PP) from CAPRES using a 10 μm pitch and the non-contact, optical sheet resistance and leakage measurement (RsL) tool from Frontier Semiconductor. A comparison is made to more conventional, i.e. penetrating, tools, such as conventional four point probe (FPP) and Variable Probe Spacing (VPS).

INTRODUCTION

The sheet resistance of source/drain and extension implants is one of the crucial parameters for optimal CMOS transistor performance. Today, there is need to accurately characterize sub-20 nm junction isolated layers, in fact, the ITRS05 roadmap calls for sub-10 nm junctions for high-performance logic in the 2007 timeframe [1]. Earlier work has illustrated that one needs to be very careful with the interpretation of conventional four point probe measurements for such shallow layers, especially in the presence of medium (well) and highly doped (halo) underlying layers, as probe penetration and junction leakage can cause very serious distortions (lowering) of the observed values due to substrate shorting [2]. One commonly used solution is to introduce a deep probe junction implant, which is doped low enough as not to influence the sheet resistance of the investigated source/drain implant, while pushing the electrical junction deep enough into the sample as to limit substrate shorting. This approach, however, requires additional processing steps. On the other hand, it has been shown before that reducing the penetration of the probes to virtually zero tends to increase the measured sheet resistance values considerably on lowly doped substrates [3] bringing them closer to their

expected values. In this work we study into more detail the behavior of three recently developed zero-penetration and/or non-contact tools both on medium and lowly doped substrates and compare them with conventional means.

STRUCTURES

For this purpose two batches (structures 3.* and 5.*) of low temperature Chemical Vapor Deposited (CVD) [4] Boron doped layers have been grown with a dopant level of about $2x10^{19}$ at/cm^3 and with thicknesses ranging from 132 down to 2 nm (table I). The Reduced Pressure Chemical Vapor Deposition (RP-CVD) system used in this work is a standard ASM Epsilon 2000 production epi reactor. This tool is a horizontal, cold wall, single wafer, load locked reactor with a lamp heated graphite susceptor in a quartz tube. Epitaxial layers were deposited on blanket 200 mm (001) Si wafers. Before deposition, the wafers received a clean in a diluted NH_4OH/O_3 solution. The native oxide was removed by an in-situ bake.

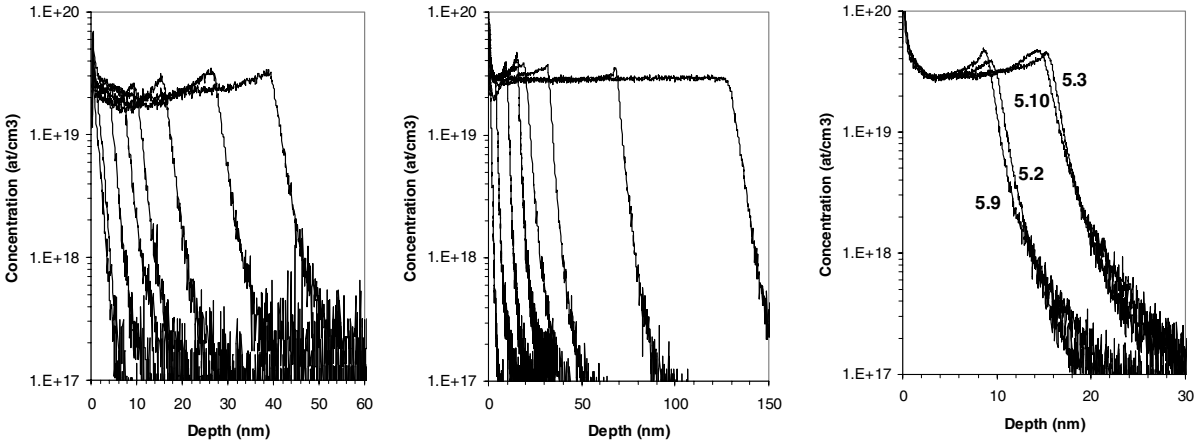

Figure 1: SIMS Boron dopant profiles (table I): (a) Batch 1 (Series 3.*) (b) Batch 2 (Series 5.*) (c) Similar profiles on medium and lowly doped substrate

Table I: Characteristics of the CVD structures used and their theoretical (SIMS-based) and experimental sheet resistances in the center, within half-radius or near the border of the wafer

Structure name	Xj at 1e19 SIMS (nm)	dopant level (at/cm3)	Substrate level (at/cm3)	Sheet resistance (Ohm/sq)									
				Theory border	RS75 border	RS75 center	VPS border	VPS center	RsL/Imec border	RsL/Imec center	RsL/FSM center	M4PP center	EMP half-radius
3.0	1.1	2.50E+19	7.E+17	21599	14	14	44		>100000	>100000	>100000		
5.0	1.7	2.88E+19	7.E+17	14558	13	13			>100000	>100000	>100000		
3.1	1.8	2.50E+19	7.E+17	13218	14	14	38		>100000	>100000	>100000		
3.2	4.7	2.60E+19	7.E+17	6819	14	14	36		>100000	>100000	>100000		30240
5.1	4.8	3.00E+19	7.E+17	5111	13	13			>100000	>100000	>100000		
3.3	7.7	2.40E+19	7.E+17	4484	13	13	35		>100000	>100000	>100000	60384	24470
3.4	10.7	1.80E+19	7.E+17	3817	13	13	30		13919	20370	17920	26988	15585
5.2	11.2	2.90E+19	7.E+17	2777	15	15			5867	15570	28729	21516	12680
3.5	17.0	1.60E+19	7.E+17	2608	15	15	32		5105	7061	6377	6695	5461
5.3	17.1	3.18E+19	7.E+17	1746	18	18			3298	5394	5790	5249	4828
5.4	22.0	3.00E+19	7.E+17	1603	14	14			2167	3455	4135	3890	2942
3.6	28.5	1.70E+19	7.E+17	1491	19	30	85		2020	2552	2659	2958	2240
5.5	34.0	3.07E+19	7.E+17	974	12	12			1147	1605	2268	1891	1647
3.7	41.2	2.30E+19	7.E+17	970	19	47	225		1089	1519	1620	1712	1662
5.6	72.0	2.70E+19	7.E+17	506	101	212					684	711	783
5.7	132.0	2.87E+19	7.E+17	276	284	380					347	407	387
5.9	10.4	3.03E+19	1.E+15	2661	4330	7770		13182	5615	10374	13209	13136	7421
5.10	16.8	2.84E+19	1.E+15	1751	2620	4020		5074	3150	4795	4880	5335	4075

The Boron doped layers were grown at 700C, 40 Torr, with $SiCl_2H_2$ as the Si precursor and B_2H_6 (1% in H_2) as the dopant gas. Most layers were grown on top of a 20 µm thick medium doped Arsenic epilayer (about $7x10^{17}$ at/cm^3) with a sheet resistance of about 14 ohm/sq (on top of a standard n-type substrate). The n-type epilayer was grown at 1130C, 760 Torr, with TCS ($SiHCl_3$) as Si precursor and AsH_3 (0.1% in H_2) as dopant gas. Two of these Boron layers, with 10 and 15 nm nominal thickness, were also deposited directly on lowly doped substrates, in order to allow for conventional four point probe comparison. The low energy Secondary Ion Mass Spectrometry (SIMS) Boron dopant profiles for both batches are shown in figure 1.

All structures were made in duplicate in order to speed up the data collection between the different involved laboratories. It has been verified with the RsL/Imec tool (see further on) that the differences between duplicate wafers were always within 10-30 %, the worst deviations being observed for the shallowest structures. For most experimental techniques, except VPS (see further on), the results close to the center of the wafer are given. For EMP a five-point average is given taken within half the wafer radius, which due to wafer non-uniformity may result in an underestimation relative to the other techniques of about 20 %. Where available also the data near the wafer border are given. The sheet resistance maps of the zero-penetration tools had a standard deviation of about 15-25 %, with the highest values located in the center.

SHEET RESISTANCE

Based on the SIMS profiles (near the wafer border) and assuming full activation and crystalline mobilities [5] it is straight forward to calculate a theoretical lower limit for the expected sheet resistances (as shown in table I and figure 2c). Next, let us consider the sheet resistance results as obtained from a conventional four point probe tool (Omnimap RS75) and variable probe experiments (VPS) [6] performed on a qualified spreading resistance probe (SRP) tool. First, we observe a good agreement (within 25 %) between the expected theoretical sheet resistance values and the slightly higher RS75 values (near the wafer border) for the two 10/15 nm boron layers grown directly on lowly doped substrate (table I, figure 2c), as is to be expected since substrate shorting is limited in this case (see also discussion on activation further on). Also, the (near border) RS75 value on the thick 132 nm layer on top of the medium doped As layer agrees well with the theoretical estimate (within 5%). For thinner layers (less than 70 nm), however, the RS75 values decrease instead of increasing (table I, figure 2a), due to a fatal amount of substrate shorting. For the thinnest layers, the RS75 value is about 14 ohm/sq, i.e. equal to the sheet resistance of the underlying As layer.

As VPS uses a lower probe load, i.e. about 5g, one expects less probe penetration (about 5-10 nm) and hence less sheet resistance distortions than in the RS75 case. As illustrated in table I (and figure 2a), the VPS data indeed show significantly higher values than RS75 (on the medium doped As layer). However, as for the RS75 case, as one considers shallower structures, the sheet resistance values are again completely dominated by substrate shorting. Hence, RS75 and VPS can be considered to be completely useless for ultra-shallow junction (USJ) profiles in the presence of a medium/highly-doped sub-layer.

Next, let us consider the zero-penetration/non-contact techniques: (i) the elastic metal four point probe (EMP) from Solid State Measurements [7], (ii) the micro four point probe (M4PP) tool from CAPRES [8] and (iii) the sheet resistance and leakage (RsL) tool from Frontier Semiconductor [9]. EMP is a four point probe tool based on the usage of relatively large metal probes (load=25 g, contact size=30-50 µm, separation=1.8 mm), which make only an

elastic contact with the sample/wafer, i.e. are non-destructive (no imprints afterwards). Measurements were performed both with constant electric field (20 mV/mm) and constant current (0.1 mA), giving similar results. EMP has the advantage that by switching the probe head, one can also do non-destructive current-voltage (CV) measurements and extract near surface concentration information. M4PP uses a miniaturized four point probe head made with micro-machining processes, which allows access to quite small structures (contact size = 50-100 nm, separation=10 µm) with an extremely low load (~0.3 mg). The current setpoint ranged between 1 and 50 µA. Furthermore, M4PP has the intrinsic capability to measure absolute carrier depth profiles on beveled samples [10]. Finally, RsL is an optical, non-contact technique based on the principle of measuring the difference in surface photo-voltage as generated by an LED between voltage probes (2 mm separation) located about 1 mm above the wafer surface. In this work, the Imec RsL tool used a short wavelength LED and the FSM RsL tool used a different LED with a wavelength optimized for a wider range of junction depths. In addition to sheet resistance measurements, the RsL tool allows for independent extraction of junction leakage current density. The recombination current density was in the range 10^{-6} to 10^{-5} A/cm^2 for all junctions with X_j>10nm. Two of the ultra-thin epi layers, structures 5.0 and 5.1, had very high leakage levels, >10^{-2} A/cm^2, indicating essentially no p-n junction. The other structures with X_j<10 nm had leakage currents in the range of 10^{-4} to 10^{-3} A/cm^2.

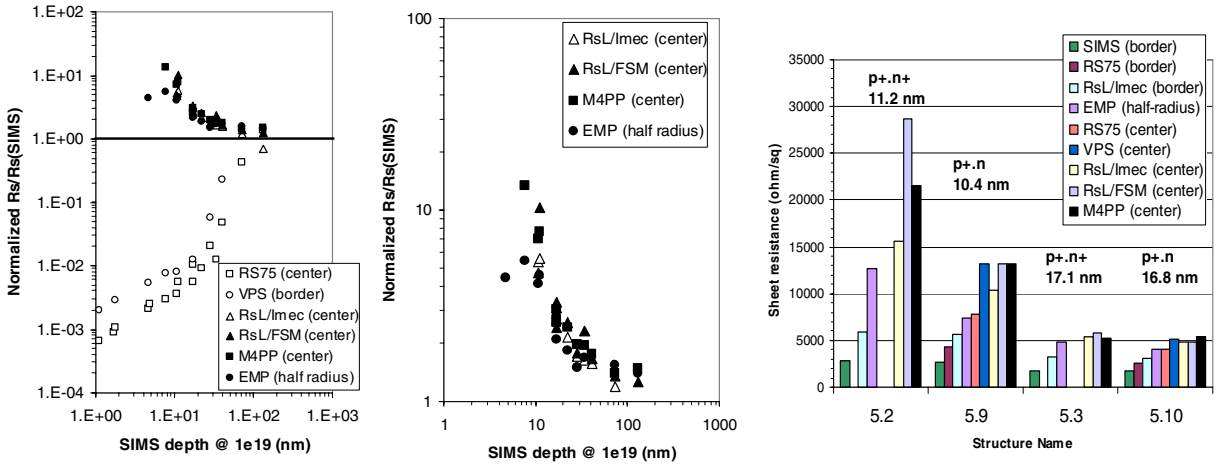

Figure 2: (a&b) Experimental sheet resistances normalized versus their theoretical value based on SIMS (c) Experimental sheet resistance for (almost) identical 10/15 nm boron layers on medium (7x10^{17} at/cm^3) and lowly doped substrate. See also table I.

Overall, all the zero-penetration techniques (EMP, M4PP, RsL) are indeed able to measure a sheet resistance on the medium doped (7x10^{17} /cm^3) sub-layer which follows the expected increasing trend as the layer thickness decreases down to 10 nm (table I). Figure 2a & 2b show the sheet resistance values as obtained by EMP (half radius) and M4PP, RsL (wafer center) normalized relative to the theoretical (SIMS) values (border). For the extremely shallow layers (less than 7.7 nm) either no value could be measured (except in one case) (M4PP, EMP) or a value higher than the maximum range (RsL) was reported. As discussed in the next section, this is, however, not a limitation of the tools themselves, but of the layers grown. A closer inspection of the data shows that the M4PP and RsL (center) values typically are the largest,

while the EMP (half-radius) ones are the smallest. The difference becomes significant for the shallowest measurable layer (7.7 nm), where it is about a factor of 3.

On the (almost) identical 15 nm layers on medium and lowly doped substrates (structures 5.3 & 5.10) (figure 2c) we observe that all techniques give results (in the center) within 30%, irrespective of the substrate. On the other hand, for the 10 nm layer on lowly doped substrate (structure 5.9) we see a factor of 2 difference (between EMP within half-radius and RsL/M4PP in the center), which increases to a factor of 4 when going to the medium doped substrate (structure 5.2), while the theoretical (border) values differ less than a few percent. It has been verified that the difference between EMP vs RsL/M4PP on structure 5.9 is not due to the usage of duplicate wafers for each structure. Dependent on the reliability one attributes to the RS75 value, one can argue that either RsL/M4PP overestimates the sheet resistance (surface states/defects/current density) or that EMP underestimates the real sheet resistance (stress effects leakage current). Based on the higher (more reliable, less penetrating) VPS result and earlier work showing an increase of the sheet resistance for decreasing probe penetration (and load) [3], the latter might be more probable. Furthermore, all techniques give a significantly higher value for the same 10 nm layer on a medium doped sublayer (structure 5.2 vs 5.9), which is opposite to what one expects. Further work will be needed to clarify the underlying physical reasons for all of these observations

DISCUSSION

Ultimately one is interested in the activation level of the involved layers. As one can see from figure 2a, the experimental non-penetrating sheet resistances deviate increasingly (towards higher ratio values) from the theoretical values for the shallower structures, indicating a lower activation for the latter ones up to the point where they start to fail. Further information can be found by plotting the inverse of the sheet resistance values versus the thickness of the respective layers taken at a SIMS dopant level of 10^{19} at/cm^3. These curves (for both batches in the center) are shown in figure 3. As the CVD layers have quite box like profiles (figure 1) their theoretical sheet resistance is approximately given by the formula: $R_s = \rho/d$, where ρ and d are respectively the layer resistivity and thickness. Hence, $1/R_s = d/\rho$, i.e. the inverse sheet resistance should be a straight line versus depth with a slope proportional with the inverse of the layer resistivity and going through the origin. As one can see from figure 3, one obtains indeed a straight line, confirming the reliability of the obtained results. The slope of these curves indicates an active concentration level (in the center) of about 1.9×10^{19} carriers/cm^3, which is about 75 % of the average SIMS dopant level (2.5×10^{19} at/cm^3 near the border).

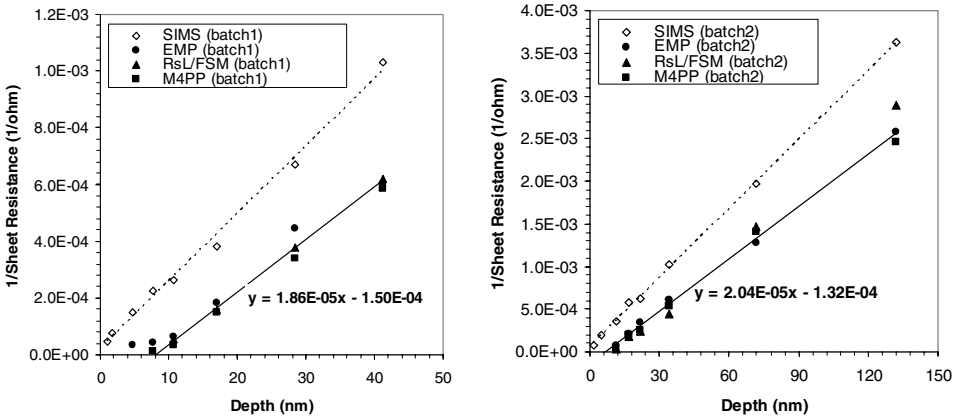

Figure 3: Inverse of sheet resistance versus layer thickness: (a) batch 1, (b) batch 2.

We observe, however, that the correlation lines in figure 3. intersect the x-axis at about 6-8 nm, i.e. they do not go through the origin. This behavior has been reported before on lowly doped substrates, for more highly doped CVD layers ($8x10^{19}$ /cm^3), where the intersection point was located at about 4-5 nm [3]. Previously, it was argued that an inactive layer of this thickness at the growth interface could be responsible for this offset, based on carrier illumination data. In this work additional information could be obtained from EMP CV measurements, which allow for the extraction of the near surface active carrier concentration levels. For all the involved CVD structures (having a p-type CV curve) a surface carrier value of about $5x10^{17}$ /cm^3 was measured, i.e. only 5 % of the total dopant concentration as given by SIMS. Consequently, it may well be that the inactive sub-layer of 5-8 nm is not located at the growth interface, but actually at the surface of the wafer. Obviously, this explains also why no sheet resistance could be measured on the sub-8 nm layers. The fact that these in fact did not have an active p-type layer on top of the underlying n-type As layer, was confirmed by CV-measurements done by the EMP tool and the shape of the modulation frequency curves in RsL. Further work is in progress to obtain high resolution (nm) carrier depth profiles with scanning spreading resistance microscopy (SSRM), scanning capacitance microscopy (SCM) and M4PP, to definitely resolve this issue.

CONCLUSIONS

The sheet resistance is a crucial technological parameter for CMOS transistor optimization. In this work the capabilities of three state-of-the-art zero-penetration sheet resistance tools has been evaluated on a series of boron doped CVD grown layers with different thicknesses both on medium and lowly doped substrates and has been compared with conventional tools such as the RS75 and VPS.

It follows that RS75 and VPS are giving useless results for sub-80 nm layers on medium ($7x10^{17}$ /cm^3) oppositely doped underlying layers. On the other hand, the results obtained by EMP, M4PP and RsL all are consistent with the characteristics of the investigated layers down to 15 nm as evidenced by the agreement with the results of the same layers on lowly doped substrates, and the analysis of their inverse sheet resistance behavior. For the shallower structures variations of up to a factor of 3 were found, which need further study.

Assuming crystalline mobility, the CVD layers grown in this work have an activation level of at least 75 % and seem to incorporate an inactive near surface sub-layer of about 6-8 nm. Further work is in progress to characterize this sub-layer into more detail.

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