ADVANCED CARRIER DEPTH PROFILING ON Si AND Ge WITH M4PP

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In order to reach the ITRS goals for future CMOS technologies there is a growing need for the accurate extraction of ultra-shallow electrically active dopant (carrier) profiles. In this work it will be illustrated that this need can be met by the micro-four point probe tool (M4PP). M4PP sheet resistance measurements taken along beveled Si and Ge blanket shallow structures will be investigated. From the differential sheet resistance changes, the underlying carrier profile can be reconstructed, without the need to rely on complicated contact modelling, i.e. M4PP carrier profiling is an absolute carrier depth profiling technique. On Si it is found that the more sensitive a structure is for the so called carrier spilling phenomenon along the bevel, the better the M4PP system performs relative to conventional SRP, due to its much lower probe pressure in combination with its sensitivity to what happens around the probes (and not underneath them). Also for Ge the same issues, change significantly the apparent carrier spilling behaviour and improve the final accuracy obtained relative to SRP.

INTRODUCTION

Recently a new approach to carrier depth profiling based on the usage of a micro-four point probe (M4PP) tool along a bevelled surface has been proposed (1). The measurement setup itself is quite similar to conventional spreading resistance probe (SRP) profiling, i.e. the micro-machined four probes (positioned at about 1.5 micron separation) are aligned with the edge of a bevelled surface and stepped down the bevel towards the substrate generating a resistance versus depth profile from which the underlying resistivity (and carrier) profile can be extracted. A major difference between M4PP and SRP is that the former gives absolute data values, i.e. there is no calibration step needed to convert the raw data towards resistivity values (1). After a smoothing step, the subsequent M4PP calculations to extract the carrier profile are extremely simple relative to the tedious SRP contact modelling approach (1).

In this work we further explore the capabilities of M4PP for carrier depth profiling. First, we discuss the impact of some experimental issues on the measurement quality, such as bevel surface roughness, starting point definition, depth resolution and reproducibility of the raw data. Next, we will mainly focus on the so called carrier spilling phenomenon for junction isolated structures. We will consider both Si-based and Ge-based diodes and compare SRP, M4PP and SSRM behaviour in the neighbourhood of the junctions.

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EXPERIMENTAL ISSUES

Previously, the required bevels were obtained through standard SRP bevelling techniques, based on mechanical polishing on a rotating roughened glass plate (2). Alternatively, SSRM based polishing techniques as used to obtained low roughness cross-sections, can also be applied for bevelling purposes (3). In this work both techniques have been used. In the future it is recommended to use only the SSRM approach, since this results in a better bevel surface with an RMS roughness of about 0.3 nm (versus about 2 nm for the SRP way). It should be noted that in practice the limiting factor is rather the peak to peak roughness than the RMS roughness. The former should ideally be less than 0.5 nm.

Previously, it was found that the determination of the starting point was not easy to do in practice on the small angles (few minutes) needed for ultra-shallow junctions profiling. As we start using SSRM bevels in stead of SRP bevels this is expected to become even more difficult due to enhanced bevel rounding of the former procedure. Hence, there is a need to systematically deposit a low temperature oxide on the samples, such that the transition from the high resistance oxide towards the low resistance semiconductor material can be determined more easily.

Figure 1 shows the raw data for different measurements on the same junction isolated structure and the corresponding extracted M4PP carrier profiles. This illustrates a good reproducibility is feasible within 10 %. It should, for completeness, be mentioned that there are still some lifetime problems with the probes (max. of 100 data points) which need further work.

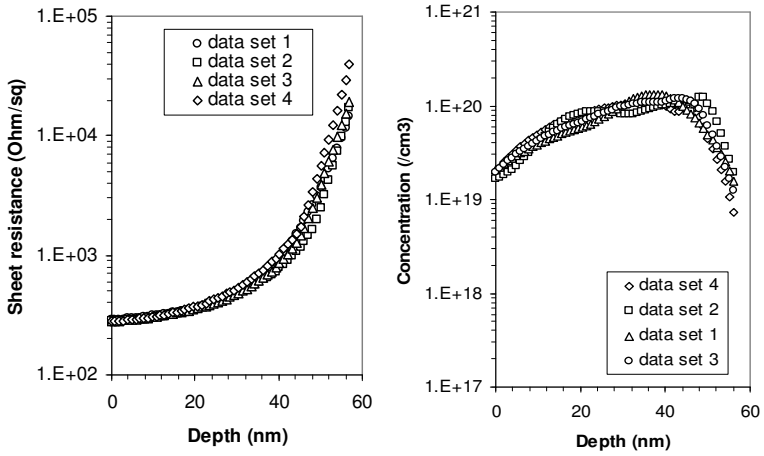

Figure 1: Repeatability of M4PP on 58 nm CVD structure: 4 measurements,(a) raw data and (b) carrier profiles. Note that the slope of the carrier profile (flat CVD profile expected) could be correlated to bevel rounding in previous work (1). SRP bevel procedure used.

The sensitivity of the tool is further illustrated by the measurements of a center and border sample taken from the same CVD grown wafer which was not as uniform as intended. As indicated in other work (4) the non uniformity was about 50%, giving a higher sheet resistance for the center piece of the wafer. Fig. 2 illustrates that the M4PP sheet resistance depth profile is indeed able to resolve these differences.

Presently a depth resolution of about 1 nm is achievable. In order to obtain this depth resolution an on bevel step size of 1 micrometer needs to be combined with a bevel angle of a few minutes. A higher depth resolution may be feasible in the near future by using etched bevels with magnifications as large as a factor of 5000 (5) leading to sub-nm depth resolution.

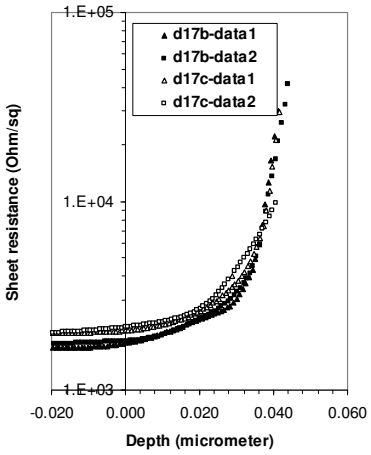

Figure 2: Sensitivity of M4PP: Raw data as obtained on the center piece D17c and border piece D17b of the same CVD grown layer (each two measurements). Smoothed data shown. SRP bevel procedure used.

For completeness it should be mentioned that with the present electronics a good electrical contact can only be established in case of a low enough contact resistance (less than 500 kOhm). The latter implies that more lowly doped profiles can not be measured at this moment. Work is in progress to improve on this situation.

When discussing the M4PP sensitivity to carrier spilling and surface roughness, it is important to realize that the area of sensitivity is fundamentally different from SRP and SSRM. Whereas SRP and SSRM are most sensitive to the resistivity directly underneath the contact point, the M4PP measures the sheet resistance in proximity of the probe position and is virtually insensitive to the sheet resistance at the contact points (6). For this reason the M4PP is highly sensitive to deep scratches (e.g. >2nm) that can result from the bevel preparation. When approaching the on-bevel electrical junction even smaller scratches (e.g. <2nm) may prevent the current to flow in a direct path between the two current probes, resulting in a sheet resistance value higher than for the ideal case consequently reducing the measured junction depth. Thus, whereas surface roughness results in noise for SRP and SSRM, it should be included in the M4PP model for completeness or ideally be reduced to zero. Finally, one must consider other geometrical effects that can occur near the on-bevel electrical junction and at the bevel starting point (7).

SILICON PROFILING

Although the mechanical depth resolution of M4PP may be adequate for structures developed in the near future, its electrical depth resolution may be worse due to the impact of the so called carrier spilling phenomenon. We discuss this issue now in more detail first for Silicon and in the next section for Germanium material.

Carrier spilling causes the on-bevel electrical carrier profile to be different from the underlying vertical carrier profile as well as from the dopant profile (assuming 100 % activation), i.e. the electrical on bevel junction, the vertical electrical junction and the metallurgical junction can all be different (2). Earlier work has illustrated that the bevel angle, probe pressure and roughness related surface state density along the bevelled surface all play a role in the amount of carrier spilling. Enhanced carrier spilling can occur under the probe contacts due to a high contact force, which locally results in significant band gap narrowing and a substantially increased dielectric constant (2). Thus, the experimental on-bevel electrical carrier profile as measured along a bevelled surface with high pressure probes may be different from the geometrically induced on-bevel carrier profile. For larger probes such as used in SRP (micrometer contact size) the pressure seems to be the dominating issue (β-tin transformation). For smaller probes as used in Scanning

Spreading Resistance Microscopy (SSRM) (using nm contact sizes), the surface states become more important (depletion/inversion layers near the surface that have an impact on the results for lowly doped regions). Here, we take a closer look at the carrier spilling behaviour of the M4PP technique (50 nm contact size).

Fig. 3a compares the SRP and M4PP carrier profiles obtained for an n^+.p 50 nm deep structure. It follows that for this rather steep profile on a lowly doped substrate (5e14 /cm^3) there is apparently little difference in carrier spilling between both techniques. On the other hand, Fig. 3b illustrates a dramatic difference for a 34 nm thick p^{++}.n^+.n structure, where the respective dopant levels were for the p^{++} layer 2e19/cm^3, for the n^+ layer 8e17/cm^3 and the n-substrate 1e15/cm^3. Where SRP suffers from a huge amount of carrier spilling pushing the electrical on bevel junction so far towards the surface that it is no longer visible, the M4PP electrical junction remains reasonably close to the metallurgical (SIMS) junction (junction depth difference of only about 9 nm). Note that this difference in carrier spilling behaviour has been observed both on bevels made with the SRP and the SSRM procedure. The measurements shown in Fig. 3b were done on a structure with a 100 nm capping oxide to obtain a precise starting point definition. This difference in apparent carrier spilling behaviour can be understood through a reduction in sensitivity due to surface roughness (scratches) close to the junction, the fact that M4PP uses lower pressure than SRP (no β-tin phase necessary) and is more sensitive to what happens in the proximity of the probes than directly underneath them.

Fig. 3c illustrates the impact of different local stress models underneath the probes through one-dimensional Poisson simulations for a 40 nm structure (using earlier developed software (8)) taking into account different vertical stress distribution through modified depth-dependent band gap and dielectric constant variations (2). The high stress carrier spilling simulations are clearly in good agreement with experimental SRP data (dominated by pressure under probes). The medium stress simulations, although resembling the experimental data, are not directly comparable to the M4PP data, because M4PP is not dominated by what happens underneath the probes (as long as the latter have near zero-penetration) but by the current flowing in between them. Actually, in theory the zero-field simulation should be the one in best correspondence with M4PP, if there were no other problems such as surface roughness. For completeness it should be mentioned that the oscillatory behaviour of the M4PP profile (Fig. 3b) is probably related with local depth variations, probe positioning and geometrical effects not yet taken into account properly (lack of topographic feed back information).

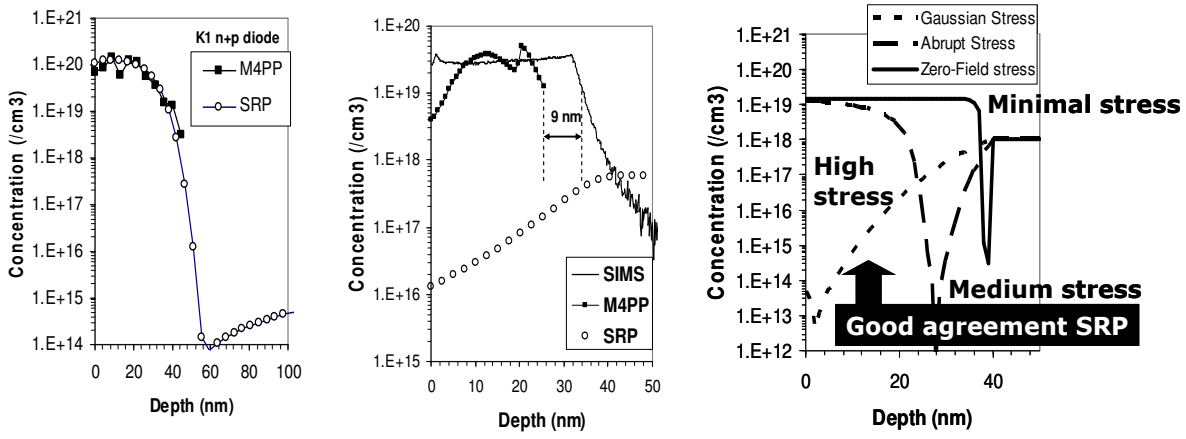

Figure 3: Comparison of SRP and M4PP on bevel carrier depth profiles with (a) similar and (b) highly different amount of carrier spilling behaviour versus (c) Poisson simulations with different stress levels for case (b). Case (a) has a lowly doped substrate (SRP bevel), while case (b) has an 8e17/cm3 doped opposite type (n-type) underlying layer (SSRM bevel). (a) without capping oxide, (b) with capping oxide.

The limited amount of carrier spilling as observed with M4PP has been confirmed on several other silicon structures not shown in this paper. One should keep in mind there will always be a minimal amount of

carrier spilling caused by the presence of the bevel, i.e. the removal of highly doped surface material as one moves down the bevel.

GERMANIUM PROFILING

Recently the interest in the carrier depth profiling of germanium implanted and annealed structures has been growing among others for improved carrier mobility reasons. Earlier we have reported on the capabilities of SRP/SSRM to profile germanium material (9). It was found that for germanium a significantly different contact model is needed relative to silicon, where a surface states distribution with a pinning level close to the top of the valence band plays an important role as illustrated in Fig. 4a. This model is able to explain why one systematically measures with SRP/SSRM a clear junction cusp on n^+.p diodes but not on p^+.n diodes (Fig. 4b). Even in the presence of a junction cusp in the SRP case, the latter very often is quite rounded and a large uncertainty exists in the precise depth location of the on bevel junction position. In the p^+.n case where the junction cusp is completely absent, it is even more difficult to pin point the junction location, or even decide whether there is actually a junction or not.

Fig. 5a compares the raw resistance data as obtained by SRP and M4PP for a P doped germanium structure (n^+.p). Immediately one can see that the on bevel junction depths (locations of maximum resistance) are very different. For M4PP the (electrical) junction depth is only 130 nm, while it is about 370 nm for SRP. Taking into account that the metallurgical (SIMS) junction in this case is at 125 nm, it is clear that the M4PP profile once again has significantly less carrier spilling than SRP. Fig. 5b shows the quantified resistivity depth profiles for M4PP and SRP. Note that the sheet resistance from the M4PP measurement is in good agreement with variable probe spacing (VPS) measurements done with SRP.

The reduced M4PP carrier spilling can most likely again be correlated with the reduced pressure of the probes. Recently we succeeded to make Transmission Electron Microscopy (TEM) cross-section images through SRP imprinted areas. As shown in Fig. 6, after removal of the SRP probes a significant amount of defects remain visible up to considerable depths (several 100 nm). The amount of defects is actually worse than in silicon (2). It can not be excluded that these defects have a non negligible impact on the carrier spilling behaviour of SRP. Up to now no such TEM images are available for the M4PP imprints (work in progress).

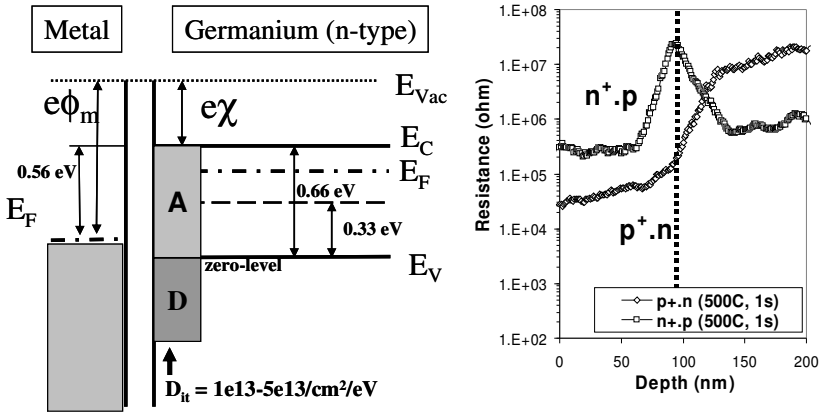

Figure 4: (a) SRP/SSRM contact model for germanium, (b) SSRM measurements illustrating the presence of a junction cusp for n+.p material but not for p+.n material (SRP has same behaviour)

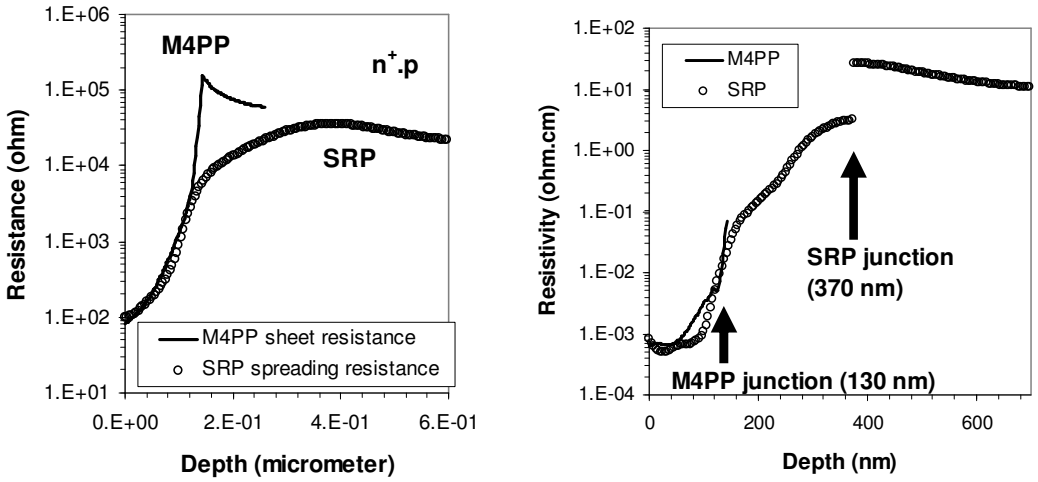

Figure 5: Comparison SRP versus M4PP raw resistance and calculated resisitivty profiles for P, 40keV, 1e15/cm2, 500C, 60 s, annealed implant into germanium (n+.p). SSRM bevel procedure.

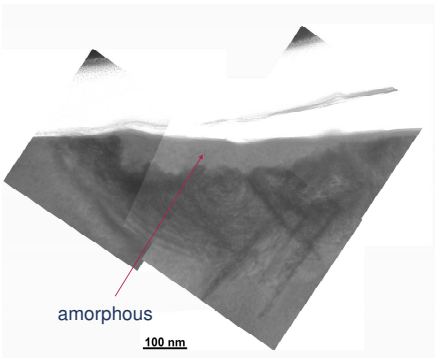

Figure 6: TEM cross-section of SRP imprint on germanium material

Fig. 7a compares the raw resistance data as obtained by SRP and M4PP for a B doped germanium structure (p+.n). Here we observe that similar to SRP/SSRM the M4PP technique does not see a junction cusp in the raw data, therefore the junction position is also difficult to localize with M4PP on p+.n structures. This is in agreement with the earlier derived germanium contact model, and can be mainly attributed to the presence of surface states (which create a thin p-type inversion layer on top of the lowly doped n-type substrate, hence apparently converting the p+.n structure close to the surface towards a p+.p structure without junction).

It follows that M4PP can be used successfully for profiling germanium structures, but that a clear junction depth determination is only possible for n+.p structures. Note that the data discussed above were obtained on samples without a capping oxide. The position of the starting point was determined through alignment of the steepest slope in the rear portion of the profile with SIMS. It is assumed that this has no impact on the basic conclusions of this work. Further work is in progress to do similar measurements on germanium structures with a capping oxide.

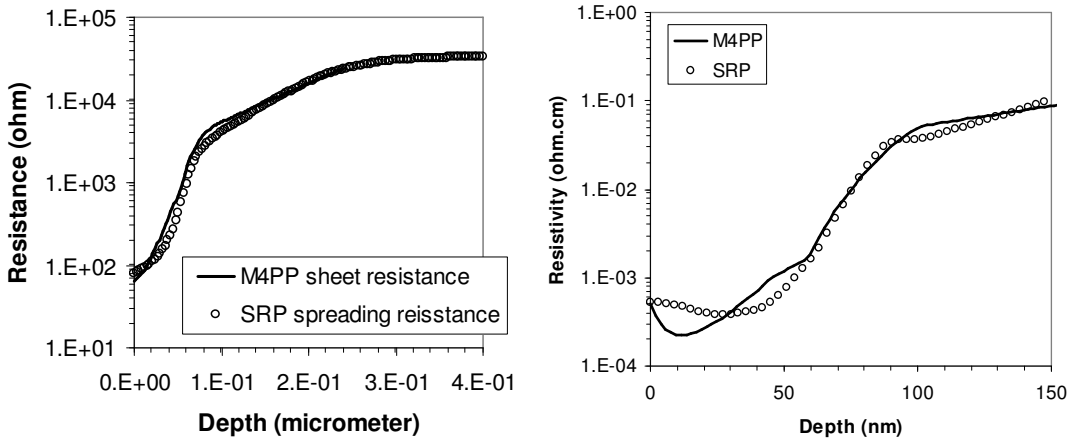

Figure 7: Comparison SRP versus M4PP raw resistance and calculated resisitivty profiles for B,4.5keV, 1e16/cm2, 500C, 60s, annealed implant into germanium (p+.n). SSRM bevel procedure.

CONCLUSIONS

There will always be a need for reliable carrier depth profiling. As SRP is running out of steam for sub-100 nm structures for many reasons, among others the problem of profile distortions due to carrier spilling, there is a need for new measurement technologies. M4PP uses a micro-machined four point-probe head (with 1.5 micrometer separations) to measure a differential sheet resistance versus depth raw data profile along a bevelled surface. Its geometrical depth resolution ultimately depends on the bevel magnifications that can be reached (sub-nm achievable).

M4PP has many advantages over SRP. First M4PP is an absolute technique, i.e. it needs no calibration samples. Furthermore, it is a virtual zero-penetration technique, it needs no probe conditioning and the calculational algorithm to extract the underlying resistivity/carrier profile is extremely simple (provided a powerful smoothing algorithm is used, and bevel rounding is avoided for example through an oxide capping layer). Also a good reproducibility and sensitivity could be observed.

Finally, due to the lower contact pressure (no β-tin and virtually zero-penetration) in combination with a sensitivity to what happens around and not underneath the probes, the amount of carrier spilling on both silicon and germanium material is found to be *significantly* less with M4PP than with SRP. The remaining apparent carrier spilling can be partially (or completely) due to a reduction of sensitivity caused by scratches (blocking the current path) close to the junction. Also geometrical effects (lateral current flow distortions near boundaries) may play a role. The impact of surface states on the results due to the bevelling process (presence/absence junction cusp on Ge diodes) can only be reduced partially by using low roughness polishing procedures (such as used for SSRM), but not completely eliminated.

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